Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.025”**

**.020 x .020”**

**.025”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .020” X .020”**

**Backside Potential:**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .025” X .025” DATE: 10/20/21**

**MFG: DIONICS THICKNESS .007” P/N: CG SERIES**

**DG 10.1.2**

#### Rev B, 7/19/02